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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,381	04/08/2004	John P. Plasterer	DATUMTE.018A	7636

20995 7590 10/17/2005

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EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 10/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/820,381	PLASTERER ET AL.	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) *5-41* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,42 and 43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/8/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4, 42-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Wang et al (US 2003/0141919)

Wang shows:

1. A circuit fabricated in an integrated circuit with a differential input and a differential output, the circuit comprising:

a differential circuit with a first NMOS transistor (M1, Fig. 11) and a second NMOS transistor (M3), where the first NMOS transistor has a source, a gate, and a drain, and the second NMOS transistor has a source, a gate, and a drain, where the source of the first NMOS transistor and the source of the second NMOS transistor are coupled, where the gate of the first NMOS transistor and the gate of the second NMOS transistor are configured to receive the differential input (VINP and VINN), and where the drain of the first NMOS transistor and the drain of the second NMOS transistor are configured to provide the differential output (at a node between transistors M1, M3 and Load);

a first current source (Itail) with at least a first terminal, where the first terminal of the first current source is coupled to the source of the first NMOS transistor and to the source of the second NMOS transistor;

a first active load (NMOS connect to M1) with at least a first terminal coupled to the drain of the first NMOS transistor of the differential circuit, where the first terminal of the first active load has an inductive impedance characteristic (page 4, [0072]) as seen from the drain of the first NMOS transistor; and

a second active load (NMOS connected to M3) coupled to the drain of the second NMOS transistor of the differential circuit, where the second active load has an inductive impedance characteristic (page 4, [0072]) as seen from the drain of the second NMOS transistor.

2. The circuit as defined in Claim 1, where the first current source is an NMOS transistor (Itail transistor is a NMOS transistor) with a source, a gate, and a drain, and where the first terminal of the first current source corresponds to the drain of the NMOS transistor.

3. The circuit as detined in Claim 1, wherein the first active load and the second active load exhibit the inductive impedance characteristic without benefit of a passive inductor (page 4, [0072]).

4. The circuit as defined in Claim 1, wherein the first active load further comprises: a third NMOS transistor (NMOS connected to M3) with a source, a gate, and a drain, where the source corresponds to the first terminal of the first active load, where the drain is coupled to a first voltage reference (VDD); and

a resistance device (R1) with a first terminal and a second terminal, where the first terminal of the resistance device is coupled to the gate of the third NMOS transistor, and where the second terminal of the resistance device is coupled to a second voltage reference (Vb).

42. An integrated circuit with metal-oxide-semiconductor field effect transistors (MOSFETs) fabricated on a silicon substrate, the integrated circuit comprising:

a differential logic circuit implemented with current controlled complementary metal-oxide semiconductor field-effect transistor (M1, M2, M3, M4) circuits; and active loads (R1 and transistors connected to R1) coupled to the transistor circuits of the differential logic circuit, where the active loads mimic the response of inductors without inclusion of an explicit inductor.

43. the integrated circuit as define in Claim 42, wherein the differential logic circuit is configured to correspond to at least a portion of a buffer (differential buffer circuit).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-F (8:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN
PRIMARY EXAMINER

10/4/05